

FIG 1

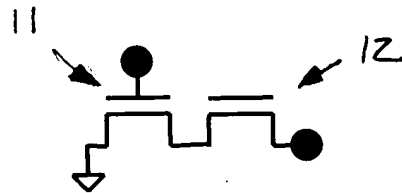


FIG 1A

SG EE	Erase	Program	Read
SG Wordline (WL)	-17V (-12V)	V_t	V_{ref}
Bitline (BL)	V_{ss} (5V)	12V	V_{dd}
Source line (SR)	V_{ss}	V_{ss}	V_{ss}

FIG 1B

FIG. 2A

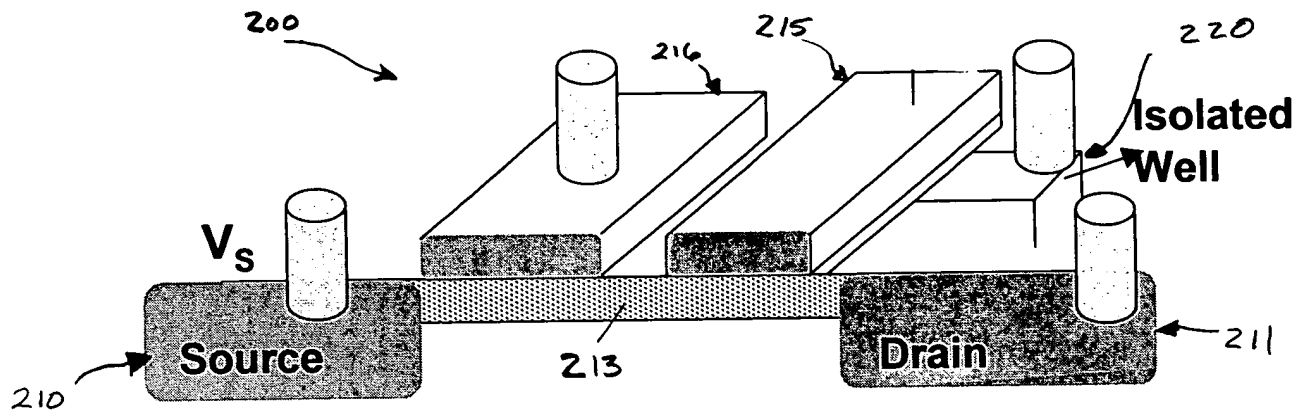
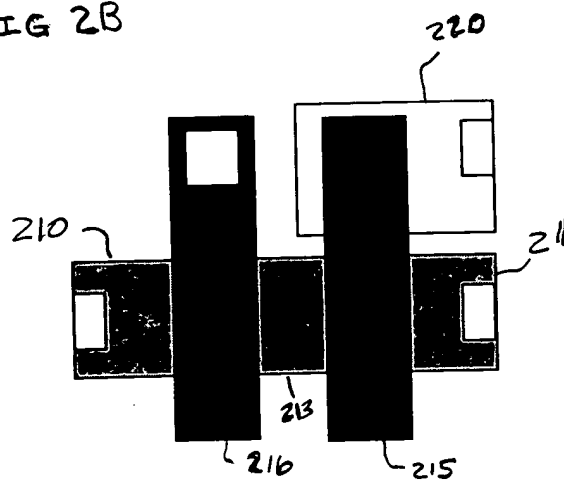


FIG. 2B



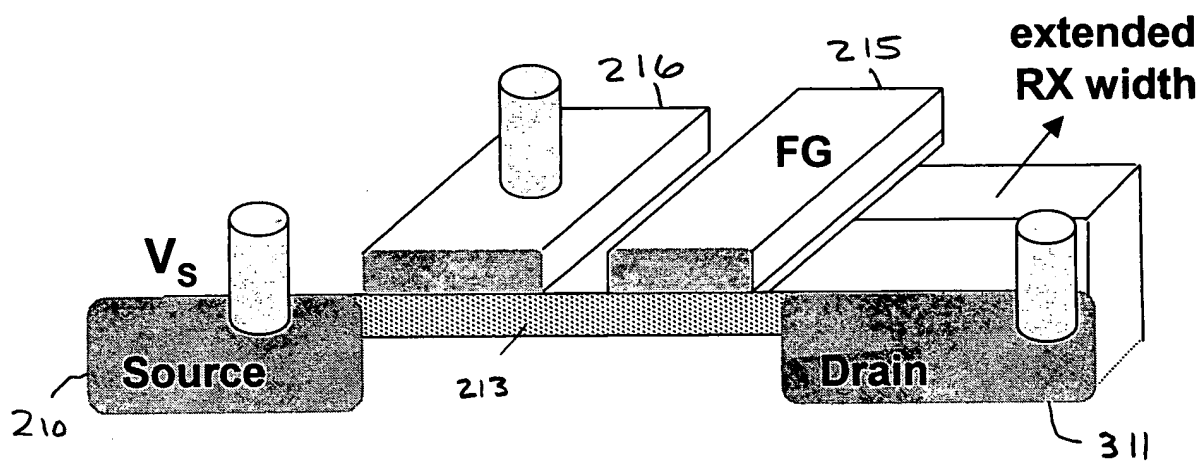


FIG 3A

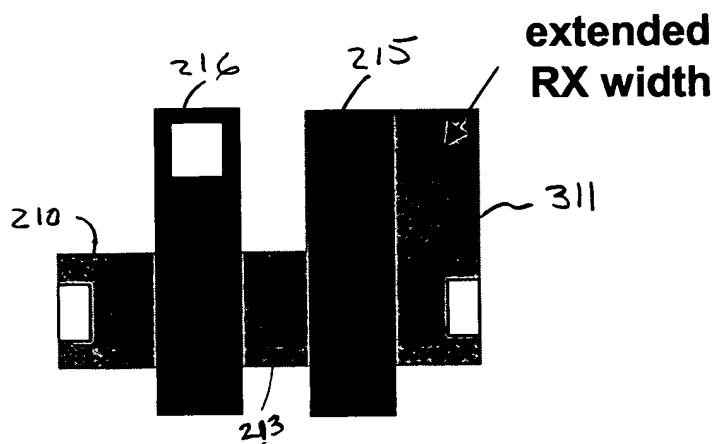
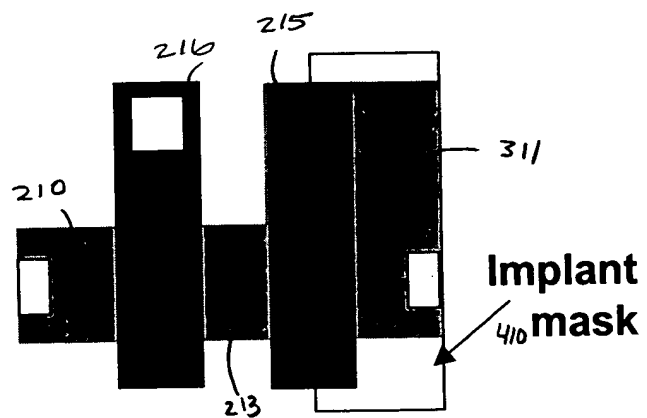
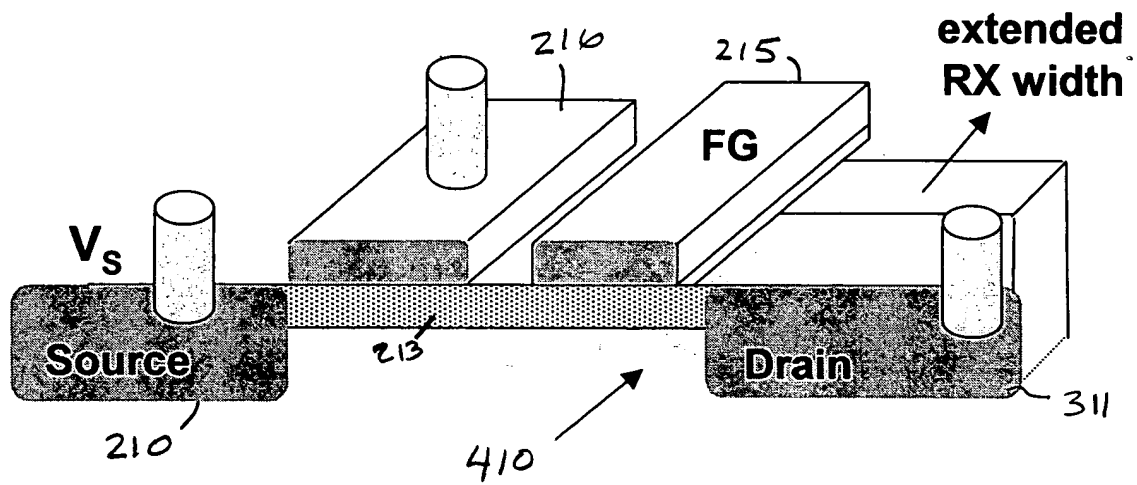


FIG 3B



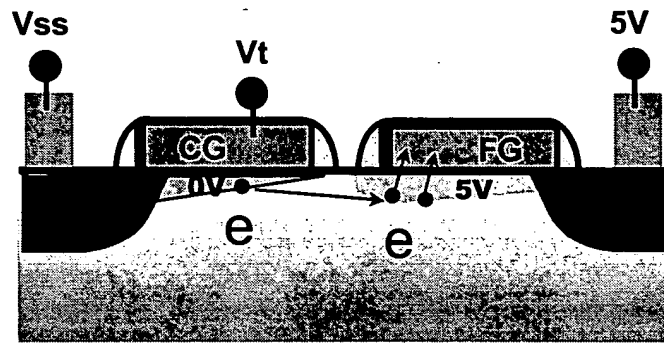
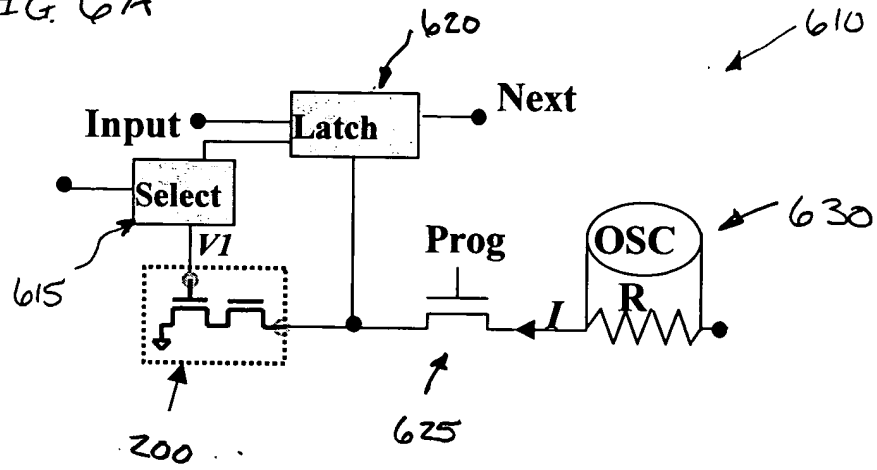


FIG 5A

NVM fuse	Erase	Program	Read
selected Wordline	-5V	V_t	V_{ref}
BL (+ iso-well)	5V	5V	V_{dd}
Source	V_{ss}	V_{ss}	V_{ss}

FIG 5B

FIG. 6A



NVM fuse	Erase	Program	Read
Select (WL)	-5V	Vt	Vref
Latch BL (Prog FET)	5V	5V (on)	Vdd (off)
Source	Vss	Vss	Vss

FIG. 6B

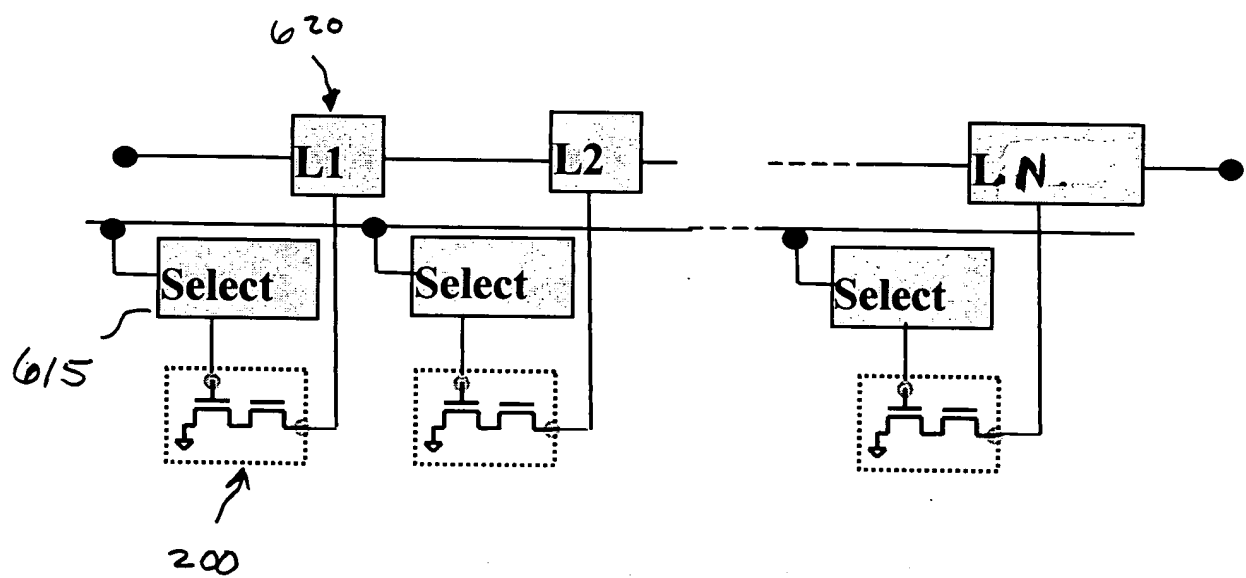


FIG. 7